TQMa35
User's Manual

TQMa35 UM 103
28.03.2013

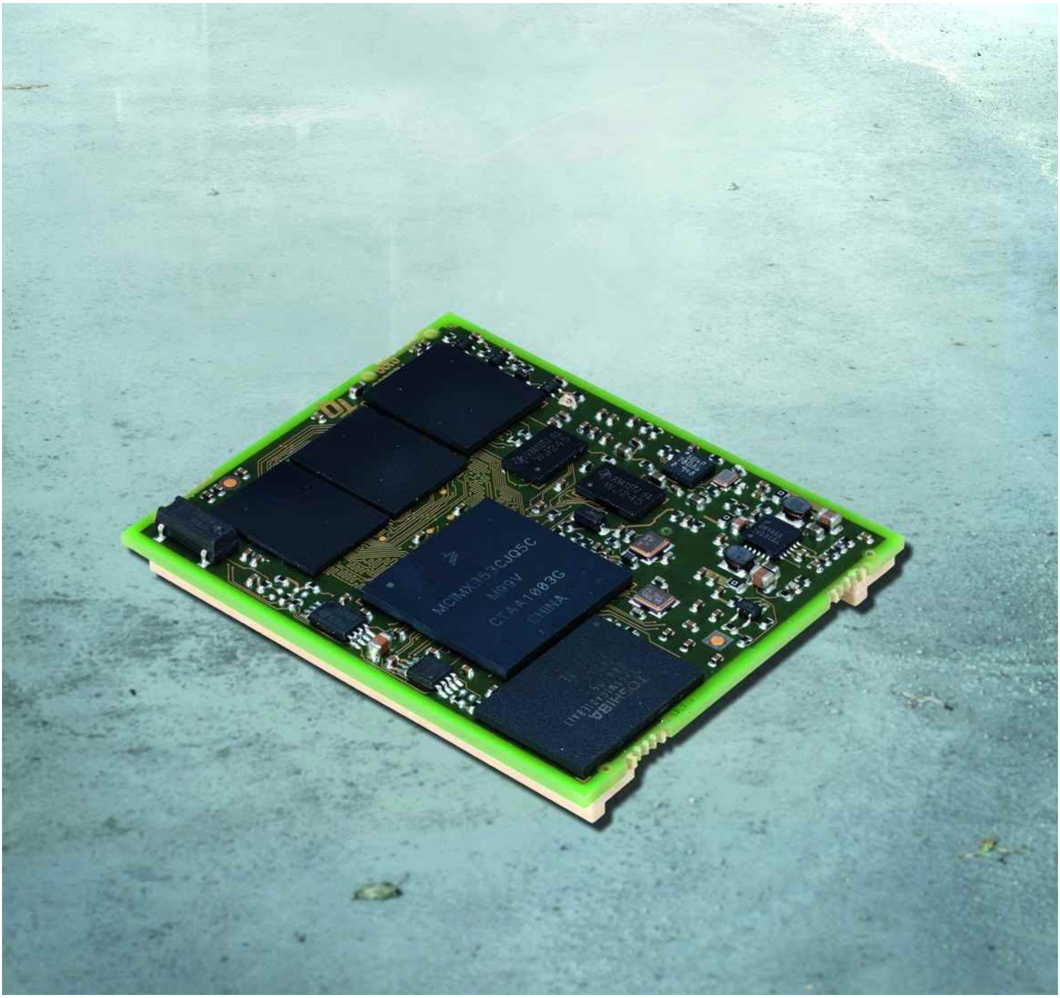


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Table directory

Illustration directory

Revision history

Rev.	Date	Name	Pos.	Modification
100	30.03.2011	Petz		Document created
101	06.12.2011	Petz	2 All 4.3.10.2 4.3.10.3 Table 4 4.3.16 Table 25 Table 25 Table 29	Power consumption corrected USB signal names corrected Syntax of signals RTS# and CTS# corrected Syntax of signals RTS# and CTS# corrected Information about gold-plating corrected Values for current consumption updated Values for current consumption updated Values for current consumption “Idle” and “Standby” added Reference (11) added
102	24.05.2012	Petz	Section 5	Link to Wiki added
103	28.03.2013	Petz	All	Typo

1. ABOUT THIS MANUAL

1.1 Copyright

1.2 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.3 Symbols and Typographic Conventions

Table 1: Terms and conventions

Symbol / Visual Cue	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	This specification is used to state the complete file name with its corresponding extension.

1.4 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the module and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

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1.6 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
82229 Seefeld
Tel: +49 (0) 8153 9308–0
Fax: +49 (0) 8153 9308–134
Email: info@tqs.de
Web: http://www.tq-group.com/

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1.8 Copyright and licence expenses

The drivers and utilities for the used components as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.
Bootloader-licence expenses are paid by TQ and are included in the price.
Licence expenses for the operating system and applications are not taken into consideration and must be separately calculated / declared.

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the used modules:**
  These documents describe the service, functionality and special characteristics of the used module (incl. BIOS).
- **Specifications of the used components:**
  The manufacturer's specifications of the used components, for example Compact-Flash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

1.10 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 2: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
ATA	Advanced Technology Attachment
BDM	Background Debug Mode
BGA	Ball Grid Array
BSP	Board Support Package
CAN	Controller Area Network
CCD	Charge-Coupled Device
CE-ATA	Consumer Electronics-Advanced Technology Attachment
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DDR	Double Data Rate
DNC	Do Not Connect
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded MultiMediaCard (Flash)
ESD	Electrostatic Discharge
FEC	Fast Ethernet Controller
FR-4	Flame Retardant-4
GPIO	General Purpose Input/Output
GPU	Graphics Processor Unit
I/O	Input/Output
IP00	Ingress Protection 00
IPU	Image Processing Unit
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
LVTTL	Low Voltage Transistor Transistor Logic
Mbps	Megabit per second
mDDR	mobile Double Data Rate
MIC	Microphone
MII	Media-Independent Interface

Table 2: Acronyms (continued)

Acronym	Meaning
MMC	Multimedia Card
MMCA	MultiMediaCard Association
MOZI	Module extractor (Modulzieher)
MSB	Most Significant Bit
MTBF	Mean operating Time Between Failures
NAND	Not-and
NC	Not Connected
NOR	Not-or
OTG	On-The-Go
PATA	Parallel ATA
PCB	Printed Circuit Board
PHY	Physical (Interface)
Ppm	Parts Per Million
PSRAM	CellularRAM ™
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input/Output
SDRAM	Synchronous Dynamic Random Access Memory
SMD	Surface-Mounted Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
UART	Universal Asynchronous Receiver/Transmitter
UL	Underwriters Laboratories Inc.
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB-HS	Universal Serial Bus - High Speed
UTMI	USB 2.0 Transceiver Macrocell Interface
WEEE	Waste Electrical and Electronic Equipment
WEIM	Wireless External Interface Module
WP	Write-Protection
WVGA	Wide Video Graphics Array (800 × 480)

2. BRIEF DESCRIPTION

The TQMa35 is a universal Minimodule with a Freescale ARM-CPU MCIMX35 (i.MX35).
The ARM1136 core works with up to 532 MHz. The module extends the TQC product range and offers a well-balanced ratio between computing performance and graphics power.
The module offers the following key functions and characteristics:

- Freescale i.MX353 (ARM11 architecture), 532 MHz
- Integrated hardware acceleration for IPU and GPU
- All functional CPU pins are routed to module connectors
- Up to 128 MiB NOR Flash
- Up to 512 MiB mDDR-SDRAM
- eMMC flash (option)
- 1 × USB 2.0 Hi-Speed Host interface
- 1 × USB 2.0 Hi-Speed OTG
- Temperature sensor
- RTC
- EEPROM
- RS232-Transceiver on-board
- Single power supply: 3.3 V
- Low power consumption (typical 1 – 1.5 W)
- Dimensions: 54 × 44 mm^2
- Easy and cost-efficient carrier board development
- Long term available

Since almost all functional pins of the processor (except SDRAM interface) are routed to the module connectors, there is a wide range of possible applications for the TQMa35.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 TQMa35 block diagram

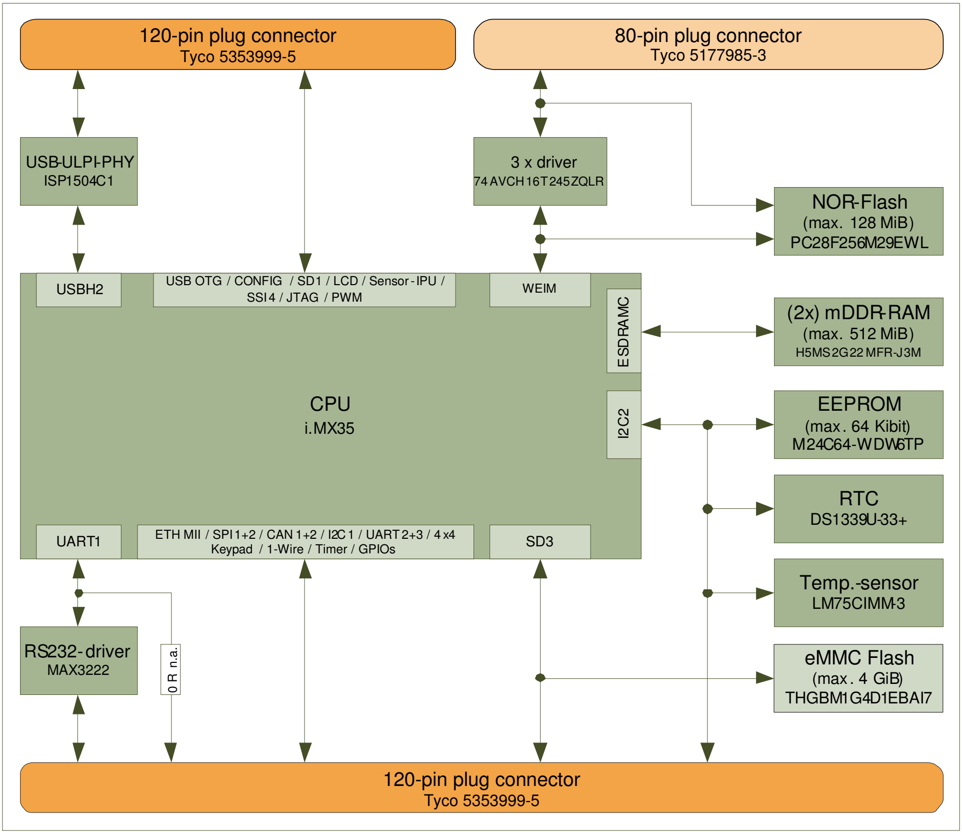


Illustration 1: TQMa35 block diagram

3.1.2 System functionality

3.1.2.1 System components

- Processor (Freescale MCIMX35, ARM1136JF-S, 532 MHz, IPU and GPU)
- Crystal oscillators for the CPU (24 MHz and 24.576 MHz)
- mDDR-SDRAM (32 Bit, 133 MHz, up to 2 devices parallel with 256 MiB each) [1]
- NOR flash (16 Bit, up to 128 MiB) [2]
- eMMC NAND flash (up to 4 GiB, SD3 interface at X1 not usable) [3]
- EEPROM (via I^2C, up to 64 Kibit) [3]
- Temperature sensor (via I^2C)
- Separate RTC (via I^2C, battery buffering possible)
- Crystal oscillator for RTC (32.768 kHz)
- RS232 driver (at UART1, RxD and TxD)
- USB-ULPI-PHY (Hi-Speed)
- Level converter (3.3 V VCCI/O for all signals at the module connectors)
- Power Management (Power-Up sequencing, voltage supervision,
  Boot mode configuration, Reset)

3.1.2.2 Interfaces

- 2 × 120-pin module connector
- 1 × 80-pin module connector [3]

A detailed overview of all available user interfaces can be found in section 4.1 on page 10.

3.1.2.3 Diagnosis LED

- Indication of reset condition

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[1] Size of mDDR-SDRAM depends on placement option.
[2] Size of NOR-Flash depends on placement option.
[3] Depends on placement option.

4. ELECTRONICS SPECIFICATION

4.1 Interfaces to other systems and devices

The TQMa35 is connected to the carrier board with 240 pins on two module connectors, optionally with 320 pins on three connectors.
The module is held in the connectors with a considerable retention force.
To avoid damaging the modules' connectors as well as the carrier board connectors while removing the module the use of an extraction tool is strongly recommended. (For more information, see section 6.3 on page 50).

4.1.1 Module connectors

Table 3: Module connectors used on the TQMa35

Manufacturer / Part No.	Description
tyco / 5353999-5	– 120-pin connector – 0.8 mm pitch – vertical – –40 °C to +85 °C
tyco [4] / 5177985-3	– 80- pin connector – 0.8 mm pitch – vertical – –40 °C to +85 °C

The following table shows suitable mating connectors for the carrier board.

[4] Depends on placement option.

Table 4: Suitable carrier board mating connectors

Manufacturer	Part No.	No. of pins	Plating	Board to board distance (see Illustration 18)
tyco	5177986-5	120	0.2 µm Gold	5 mm
tyco	5-5177986-5	120	0.76 µm Gold	5 mm
tyco	1-5177986-5	120	0.2 µm Gold	6 mm
tyco	6-5177986-5	120	0.76 µm Gold	6 mm
tyco	2-5177986-5	120	0.2 µm Gold	7 mm
tyco	--------------	120	0.76 µm Gold	7 mm
tyco	3-5177986-5	120	0.2 µm Gold	8 mm
tyco	6123001-5	120	0.76 µm Gold	8 mm
tyco	5177986-3	80	0.2 µm Gold	5 mm
tyco	5-5177986-3	80	0.76 µm Gold	5 mm
tyco	1-5177986-3	80	0.2 µm Gold	6 mm
tyco	6-5177986-3	80	0.76 µm Gold	6 mm
tyco	2-5177986-3	80	0.2 µm Gold	7 mm
tyco	--------------	80	0.76 µm Gold	7 mm
tyco	3-5177986-3	80	0.2 µm Gold	8 mm
tyco	6123001-3	80	0.76 µm Gold	8 mm

4.1.2 Pin assignment

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of.
The pins assignment listed in sections 4.1.2.1 to 4.1.2.3 refer to the corresponding standard BSP of TQ-Systems GmbH.

4.1.2.1 Module connector X1

Table 5: Pin assignment module connector X1

Group	Signal	I/O	X1		I/O	Signal	Group
Power	VCC3V3	P	1	2	P	VCC3V3	Power
Power	VCC3V3	P	3	4	P	VCC3V3	Power
Power	VCC3V3	P	5	6	P	VCC3V3	Power
Power	VCC3V3	P	7	8	P	VCC3V3	Power
Power	VBAT	P	9	10	P	DGND	Power
Power	DGND	P	11	12	P	DGND	Power
General clock	CLKO	O	13	14	P	DGND	Power
Power	DGND	P	15	16	P	DGND	Power
GPIO	GPIO1_4	I/O	17	18	P	DGND	Power
	GPIO1_5	I/O	19	20	I/O	GPIO1_12	GPIO
Power	DGND	P	21	22	I/O	GPIO1_22	
GPIO	GPIO2_7	I/O	23	24	I/O	GPIO2_0	
	GPIO2_18	I/O	25	26	P	DGND	Power
	GPIO2_23	I/O	27	28	I/O	COL0	4x4 keypad
	GPIO2_25	I/O	29	30	I/O	COL1	
Power	DGND	P	31	32	I/O	COL2	
4x4 keypad	ROW0	I/O	33	34	I/O	COL3	
	ROW1	I/O	35	36	P	DGND	Power
	ROW2	I/O	37	38	I/O	GPIO3_3	GPIO
	ROW3	I/O	39	40	I/O	GPIO3_4	
Power	DGND	P	41	42	I/O	GPIO3_5	
1-Wire	OWDAT	I/O	43	44	I/O	SPI2_SS0	SPI 2
SPI 1	SPI1_SS0	I/O	45	46	P	DGND	Power
	SPI1_SS1	I/O	47	48	I/O	SPI2_CLK	SPI 2
	SPI1_SS3	I/O	49	50	I/O	SPI2_MISO	
Power	DGND	P	51	52	I/O	SPI2_MOSI	
SPI 1	SPI1_CLK	I/O	53	54	I	SPI2_RDY	
	SPI1_MISO	I/O	55	56	P	DGND	Power
	SPI1_MOSI	I/O	57	58	I/O	I2C1_SCL	I²C 1
	SPI1_RDY	I	59	60	I/O	I2C1_SDA	
Power	DGND	P	61	62	I/O	I2C2_SCL	I²C 2
Timer	TIM_CAPIN1	I	63	64	I/O	I2C2_SDA	
	TIM_CMPOUT1	O	65	66	P	DGND	Power
SD card 3	SD3_CMD	I/O	67	68	I/O	SD3_DAT0	SD card 3
	SD3_CLK	O	69	70	I/O	SD3_DAT1	
Power	DGND	P	71	72	I/O	SD3_DAT2	
SD card 3	SD3_DAT4	I/O	73	74	I/O	SD3_DAT3	
	SD3_DAT5	I/O	75	76	P	DGND	Power
	SD3_DAT6	I/O	77	78	O	FEC_TXD0	Ethernet MII
	SD3_DAT7	I/O	79	80	O	FEC_TXD1	
Power	DGND	P	81	82	O	FEC_TXD2	
Ethernet MII	FEC_TXD3	O	83	84	I	FEC_TX_CLK	
	FEC_TX_ER	O	85	86	P	DGND	Power
	FEC_TX_EN	O	87	88	I	FEC_RXD0	Ethernet MII
	FEC_RXD1	I	89	90	I	FEC_RXD2	
Power	DGND	P	91	92	P	DGND	Power
Ethernet MII	FEC_RXD3	I	93	94	I	FEC_RX_CLK	Ethernet MII
	FEC_RX_ER	I	95	96	P	DGND	Power
	FEC_RX_DV	I	97	98	I/O	FEC_MDIO	Ethernet MII
	FEC_MDC	O	99	100	I	FEC_CRS	
Power	DGND	P	101	102	I	FEC_COL	
CAN 2	CAN2_TX	O	103	104	I	CAN2_RX	CAN 2
CAN 1	CAN1_TX	O	105	106	P	DGND	Power
	CAN1_RX	I	107	108	I	UART3_RTS#	UART 3
UART 3	UART3_CTS#	O	109	110	O	UART3_TXD	
Power	DGND	P	111	112	I	UART3_RXD	
UART 2	UART2_RTS#	I	113	114	O	UART2_CTS#	UART 2
	UART2_TXD	O	115	116	P	DGND	Power
	UART2_RXD	I	117	118	O	RS232_TXD	RS232
Power	DGND	P	119	120	I	RS232_RXD	

4.1.2.2 Module connector X2

Table 6: Pin assignment module connector X2

Group	Signal	I/O				I/O	Signal	Group
Power	DGND	P	1		2	I	FLASH_RESET#	NOR-Flash-CTRL
Reserve	NC	-	3		4	I	WP#_ACC	
	NC	-	5		6	P	DGND	Power
Power Management	VSTBY	I	7		8	I	WDOG_RST#	Reset
Timer	PWM	O	9		10	I	JTAG_RESET#	
Power	DGND	P	11		12	I	RESET_IN#	
SSI 4	SSI_TXD	I/O	13		14	O	POR#	
	SSI_RXD	I/O	15		16	P	DGND	Power
	SSI_TXC	I/O	17		18	O	LD0	IPU-LCD
	SSI_TXFS	I/O	19		20	O	LD1	
Power	DGND	P	21		22	O	LD2	
IPU-LCD	LD3	O	23		24	O	LD4	
	LD5	O	25		26	P	DGND	Power
	LD7	O	27		28	O	LD6	IPU-LCD
	LD9	O	29		30	O	LD8	
Power	DGND	P	31		32	O	LD10	
IPU-LCD	LD11	O	33		34	O	LD12	
	LD13	O	35		36	P	DGND	Power
	LD15	O	37		38	O	LD14	IPU-LCD
	LD17	O	39		40	O	LD16	
Power	DGND	P	41		42	O	LD18	
IPU-LCD	LD19	O	43		44	O	LD20	
	LD21	O	45		46	P	DGND	Power
	LD23	O	47		48	O	LD22	IPU-LCD
	LD_DRDY	O	49		50	O	LD_SPL	
Power	DGND	P	51		52	O	LD_REV	
IPU-LCD	LD_HSYNC	O	53		54	O	LD_CLS	
	LD_VSYNC	O	55		56	P	DGND	Power
Power	DGND	P	57		58	O	LD_CONTRAST	IPU-LCD
IPU-LCD	LD_CLK	O	59	X2	60	I	USBHS_OC	USB Host Hi-Speed
Power	DGND	P	61		62	O	USBHS_PSW#	
USB Host Hi-Speed	USBHS_UID	I	63		64	I/O	USBHS_VBUS	
Power	DGND	P	65		66	P	DGND	Power
USB Host Hi-Speed	USBHS_UDP	I/O	67		68	I	USB_OTG_OC	USB OTG Hi-Speed
	USBHS_UDM	I/O	69		70	O	USB_OTG_PWR	
Power	DGND	P	71		72	I	USB_OTG_UID	
USB OTG Hi-Speed	USB_OTG_DM	I/O	73		74	I/O	USB_OTG_VBUS	
	USB_OTG_DP	I/O	75		76	P	DGND	Power
Power	DGND	P	77		78	I/O	SD1_DAT0	SD card 1
SD card 1	SD1_CLK	O	79		80	I/O	SD1_DAT1	
Power	DGND	P	81		82	I/O	SD1_DAT2	
SD card 1	SD1_CMD	I/O	83		84	I/O	SD1_DAT3	
IPU-CSI	CSI_D1	I	85		86	P	DGND	Power
	CSI_D3	I	87		88	I	CSI_D0	IPU-CSI
	CSI_D5	I	89		90	I	CSI_D2	
Power	DGND	P	91		92	I	CSI_D4	
IPU-CSI	CSI_D7	I	93		94	I	CSI_D6	
	CSI_D9	I	95		96	P	DGND	Power
	CSI_D11	I	97		98	I	CSI_D8	IPU-CSI
	CSI_D13	I	99		100	I	CSI_D10	
Power	DGND	P	101		102	I	CSI_D12	
IPU-CSI	CSI_D15	I	103		104	I	CSI_D14	
	CSI_VSYNC	I	105		106	P	DGND	Power
	CSI_HSYNC	I	107		108	O	CSI_MCLK	IPU-CSI
	CSI_PIXCLK	I	109		110	I/O	DE#	CPU-JTAG
Power	DGND	P	111		112	O	RTCK	
CPU-JTAG	TCK	I	113		114	I	JTAG_MOD	
	TMS	I	115		116	P	DGND	Power
	TDI	I	117		118	O	TDO	CPU-JTAG
Power	DGND	P	119		120	I	TRST#	

4.1.2.3 Module connector X3

Table 7: Pin assignment module connector X3

Group	Signal	I/O				I/O	Signal	Group
Power	DGND	P	1		2	I/O	D0	16 bit data bus
16 bit data bus	D1	I/O	3		4	I/O	D2	
	D3	I/O	5		6	P	DGND	Power
	D5	I/O	7		8	I/O	D4	16 bit data bus
	D7	I/O	9		10	I/O	D6	
Power	DGND	P	11		12	I/O	D8	
16 bit data bus	D9	I/O	13		14	I/O	D10	
	D11	I/O	15		16	P	DGND	Power
	D13	I/O	17		18	I/O	D12	16 bit data bus
	D15	I/O	19		20	I/O	D14	
Power	DGND	P	21		22	O	A0	26 bit address bus
26 bit address bus	A1	O	23		24	O	A2	
	A3	O	25		26	P	DGND	Power
	A5	O	27		28	O	A4	26 bit address bus
	A7	O	29		30	O	A6	
Power	DGND	P	31		32	O	A8	
26 bit address bus	A9	O	33		34	O	A10	
	A11	O	35		36	P	DGND	Power
	A13	O	37		38	O	A12	26 bit address bus
	A15	O	39	X3	40	O	A14	
Power	DGND	P	41		42	O	A16	
26 bit address bus	A17	O	43		44	O	A18	
	A19	O	45		46	P	DGND	Power
	A21	O	47		48	O	A20	26 bit address bus
	A23	O	49		50	O	A22	
Power	DGND	P	51		52	O	A24	
26 bit address bus	A25	O	53		54	O	LBA#	Bus-CTRL
Bus-CTRL	DTACK#	I	55		56	P	DGND	Power
Power	DGND	P	57		58	O	RW#	Bus-CTRL
Bus-CTRL	BUS_CLK	O	59		60	O	OE#	
Power	DGND	P	61		62	I	ECB#	
Bus-CTRL	EB1#	O	63		64	O	EB0#	
	CS1#	O	65		66	P	DGND	Power
	CS5#	O	67		68	-	DNC	Factory test only
Factory test only	DNC	-	69		70	-	DNC	
Power	DGND	P	71		72	-	DNC	
Factory test only	DNC	-	73		74	-	DNC	
	DNC	-	75		76	P	DGND	Power
	DNC	-	77		78	-	NC	Reserve
Power	DGND	P	79		80	-	NC	

4.1.3 Pin description

The pins of the module connectors are described in detail in the following tables.
External and internal pull-up or-down wirings as well as the references to I/O voltage and processor pin characteristics are listed in addition to direction, pin name and pin number.

The processor pin in parentheses () means there is no direct connection between processor and connector (e.g. via level converter) or that connector and processor are connected to the output simultaneously.

Attention: Pin characteristics	
	The entries in Table 8 to Table 10 for direction, internal pull/keeper, slew rate and drive strength are values for the standard-BSP of TQ-Systems GmbH and can also be configured differently.

4.1.3.1 Module connector X1

Table 8: Pin description X1

Pin	Pin name	Direction	External pull-up / -down	i.MX35 Parameter					Remark
				VCCIO	CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
1	VIN	P		–	–	–			
2	VIN	P		–	–	–			
3	VIN	P		–	–	–			
4	VIN	P		–	–	–			
5	VIN	P		–	–	–			
6	VIN	P		–	–	–			
7	VIN	P		–	–	–			
8	VIN	P		–	–	–			
9	VBAT	P		–	–	–			See section 4.3.18 on page 48
10	DGND	P		–	–	–			
11	DGND	P		–	–	–			
12	DGND	P		–	–	–			
13	CLKO	O		$V_{i.MX35}$	V10	–	Fast	Max	
14	DGND	P		–	–	–			
15	DGND	P		–	–	–			
16	DGND	P		–	–	–			
17	GPIO1_4	I/O		$V_{i.MX35}$	K3	100 kΩ	Slow	Nom	
18	DGND	P		–	–	–			
19	GPIO1_5	I/O		$V_{i.MX35}$	K5	100 kΩ	Slow	Nom	
20	GPIO1_12	I/O		$V_{i.MX35}$	J2	100 kΩ	Slow	Nom	Optional interrupt signal of RTC
21	DGND	P		–	–	–			
22	GPIO1_22	I/O		$V_{i.MX35}$	G3	–	Fast	Nom	Optional overtemperature signal of temperature sensor
23	GPIO2_7	I/O		$V_{i.MX35}$	T7	–	Slow	Nom	
24	GPIO2_0	I/O		$V_{i.MX35}$	U11	Keeper	Slow	Nom	
25	GPIO2_18	I/O		$V_{i.MX35}$	W4	100 kΩ	Slow	Nom	
26	DGND	P		–	–	–			
27	GPIO2_23	I/O		$V_{i.MX35}$	F3	100 kΩ	Fast	Nom	
28	COL0	I/O		$V_{i.MX35}$	H5	100 kΩ	Slow	Nom	
29	GPIO2_25	I/O		$V_{i.MX35}$	U3	100 kΩ	Slow	Nom	
30	COL1	I/O		$V_{i.MX35}$	H1	100 kΩ	Slow	Nom	
31	DGND	P		–	–	–			

Table 8: Pin description X1 (continued)

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	Remark
32	COL2	I/O		$V_{i.MX35}$	G4	100 kΩ	Slow	Nom	
33	ROW0	I/O		$V_{i.MX35}$	W1	100 kΩ	Slow	Nom	
34	COL3	I/O		$V_{i.MX35}$	J5	100 kΩ	Slow	High	
35	ROW1	I/O		$V_{i.MX35}$	T4	100 kΩ	Slow	Nom	
36	DGND	P		–	–	–			
37	ROW2	I/O		$V_{i.MX35}$	J4	100 kΩ	Slow	Nom	
38	GPIO3_3	I/O		$V_{i.MX35}$	W13	100 kΩ	Fast	Nom	
39	ROW3	I/O		$V_{i.MX35}$	J1	100 kΩ	Slow	Nom	
40	GPIO3_4	I/O		$V_{i.MX35}$	Y13	100 kΩ	Fast	Nom	
41	DGND	P		–	–	–			
42	GPIO3_5	I/O		$V_{i.MX35}$	W12	100 kΩ	Fast	Nom	
43	OWDAT	I/O		$V_{i.MX35}$	T11	Keeper	Slow	Nom	
44	SPI2_SS0	I/O		$V_{i.MX35}$	K2	100 kΩ	Slow	High	
45	SPI1_SS0	I/O		$V_{i.MX35}$	Y8	100 kΩ	Slow	Nom	
46	DGND	P		–	–	–			
47	SPI1_SS1	I/O		$V_{i.MX35}$	U8	100 kΩ	Slow	Nom	
48	SPI2_CLK	I/O		$V_{i.MX35}$	L5	100 kΩ	Slow	Nom	
49	SPI1_SS3	I/O		$V_{i.MX35}$	V7	–	Slow	Nom	
50	SPI2_MISO	I/O		$V_{i.MX35}$	K4	100 kΩ	Slow	Nom	
51	DGND	P		–	–	–			
52	SPI2_MOSI	I/O		$V_{i.MX35}$	K1	100 kΩ	Slow	Nom	
53	SPI1_CLK	I/O		$V_{i.MX35}$	W8	100 kΩ	Slow	Nom	
54	SPI2_RDY	I		$V_{i.MX35}$	J6	100 kΩ	Slow	Nom	
55	SPI1_MISO	I/O		$V_{i.MX35}$	V9	100 kΩ	Slow	Nom	
56	DGND	P		–	–	–			
57	SPI1_MOSI	I/O		$V_{i.MX35}$	W9	100 kΩ	Slow	Nom	
58	I2C1_SCL	I/O_{OD}	1.2 kΩ	$V_{i.MX35}$	M20	100 kΩ	Slow	Nom	
59	SPI1_RDY	I		$V_{i.MX35}$	T8	100 kΩ	Slow	Nom	
60	I2C1_SDA	I/O_{OD}	1.2 kΩ	$V_{i.MX35}$	N17	100 kΩ	Slow	Nom	
61	DGND	P	–	–	–				
62	I2C2_SCL	I/O_{OD}	1.2 kΩ	$V_{i.MX35}$	L3	100 kΩ	Slow	Nom	
63	TIM_CAPIN1	I		$V_{i.MX35}$	V12	100 kΩ	Slow	Nom	
64	I2C2_SDA	I/O_{OD}	1.2 kΩ	$V_{i.MX35}$	M1	100 kΩ	Slow	Nom	
65	TIM_CMPOUT1	O	–	$V_{i.MX35}$	T12	100 kΩ	Slow	Nom	

Table 8: Pin description X1 (continued)

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
66	DGND	P	–	–	–				
67	SD3_CMD	I/O	10 kΩ [5]	$V_{i.MX35}$	Y4	100 kΩ	Slow	Nom	Do not connect when eMMC is assembled
68	SD3_DAT0	I/O	10 kΩ [5]	$V_{i.MX35}$	Y6		Slow	Nom	Do not connect when eMMC is assembled
69	SD3_CLK	O		$V_{i.MX35}$	U5	100 kΩ	Slow	Nom	Do not connect when eMMC is assembled
70	SD3_DAT1	I/O	10 kΩ [5]	$V_{i.MX35}$	W6		Slow	Nom	Do not connect when eMMC is assembled
71	DGND	P	–	–	–				
72	SD3_DAT2	I/O	10 kΩ [5]	$V_{i.MX35}$	V6		Slow	Nom	Do not connect when eMMC is assembled
73	SD3_DAT4	I/O	10 kΩ [5]	$V_{i.MX35}$	U6	100 kΩ	Slow	Nom	Do not connect when eMMC is assembled
74	SD3_DAT3	I/O	10 kΩ [5]	$V_{i.MX35}$	T6		Slow	Nom	Do not connect when eMMC is assembled
75	SD3_DAT5	I/O	10 kΩ [5]	$V_{i.MX35}$	Y5	100 kΩ	Slow	Nom	Do not connect when eMMC is assembled
76	DGND	P	–	–	–				
77	SD3_DAT6	I/O	10 kΩ [5]	$V_{i.MX35}$	W5	100 kΩ	Slow	Nom	Do not connect when eMMC is assembled
78	FEC_TXD0	O	–	$V_{i.MX35}$	P5		Slow	Nom	
79	SD3_DAT7	I/O	10 kΩ [5]	$V_{i.MX35}$	V5	100 kΩ	Slow	Nom	Do not connect when eMMC is assembled
80	FEC_TXD1	O		$V_{i.MX35}$	M4	–	Slow	Nom	
81	DGND	P		–	–	–			
82	FEC_TXD2	O		$V_{i.MX35}$	M5	–	Slow	Nom	
83	FEC_TXD3	O		$V_{i.MX35}$	L6	–	Slow	Nom	
84	FEC_TX_CLK	I		$V_{i.MX35}$	P4	100 kΩ	Slow	Nom	
85	FEC_TX_ER	O		$V_{i.MX35}$	N4	–	Slow	Nom	
86	DGND	P		–	–	–			
87	FEC_TX_EN	O		$V_{i.MX35}$	T1	–	Slow	Nom	
88	FEC_RXD0	I		$V_{i.MX35}$	P2	100 kΩ	Slow	Nom	

[5] Pull-up only assembled when eMMC is assembled.

Table 8: Pin description X1 (continued)

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
89	FEC_RXD1	I		$V_{i.MX35}$	N2	100 kΩ	Slow	Nom	
90	FEC_RXD2	I		$V_{i.MX35}$	M3	100 kΩ	Slow	Nom	
91	DGND	P		–	–	–			
92	DGND	P		–	–	–			
93	FEC_RXD3	I		$V_{i.MX35}$	N1	100 kΩ	Slow	Nom	
94	FEC_RX_CLK	I		$V_{i.MX35}$	R2	100 kΩ	Slow	Nom	
95	FEC_RX_ER	I		$V_{i.MX35}$	N3	100 kΩ	Slow	Nom	
96	DGND	P		–	–	–			
97	FEC_RX_DV	I		$V_{i.MX35}$	T2	100 kΩ	Slow	Nom	
98	FEC_MDIO	I/O	1.5 kΩ	$V_{i.MX35}$	P1	22 kΩ	Slow	Nom	
99	FEC_MDC	O		$V_{i.MX35}$	R1	–	Slow	Nom	
100	FEC_CRS	I		$V_{i.MX35}$	N5	100 kΩ	Slow	Nom	
101	DGND	P		–	–	–			
102	FEC_COL	I		$V_{i.MX35}$	P3	100 kΩ	Slow	Nom	
103	CAN2_TX	I/O		$V_{i.MX35}$	J3	100 kΩ	Slow	Nom	
104	CAN2_RX	I		$V_{i.MX35}$	H4	100 kΩ	Slow	Nom	
105	CAN1_TX	I/O		$V_{i.MX35}$	V4	100 kΩ	Slow	Nom	
106	DGND	P		–	–	–			
107	CAN1_RX	I/O		$V_{i.MX35}$	Y3	100 kΩ	Slow	Nom	
108	UART3_RTS#	I		$V_{i.MX35}$	U4	100 kΩ	Slow	Nom	
109	UART3_CTS#	O		$V_{i.MX35}$	W15	100 kΩ	Slow	Nom	
110	UART3_TXD	O		$V_{i.MX35}$	Y2	100 kΩ	Slow	Nom	
111	DGND	P		–	–	–			
112	UART3_RXD	I		$V_{i.MX35}$	V3	100 kΩ	Slow	Nom	
113	UART2_RTS#	I		$V_{i.MX35}$	G1	100 kΩ	Slow	Nom	
114	UART2_CTS#	O		$V_{i.MX35}$	G5	–	Slow	Nom	
115	UART2_TXD	O		$V_{i.MX35}$	H2	–	Slow	Nom	
116	DGND	P		–	–	–			
117	UART2_RXD	I		$V_{i.MX35}$	H3	100 kΩ	Slow	Nom	
118	RS232_TXD [6]	O		V_{RS232}	(R6)	–			Optionally UART1_TxD
119	DGND	P		–	–	–			
120	RS232_RXD [6]	I		V_{RS232}	(U2)	–			Optionally UART1_RxD

[6] VCCIO depends on placement option (if UART1 is used instead of RS232, then VCCIO = Vi.MX35).

4.1.3.2 Module connector X2

Table 9: Pin description X2

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
1	DGND	P	–	–	–				
2	FLASH_RESET#	I	18 kΩ	V_{NOR}	–				
3	NC	–	–	–	–				Not connected
4	WP#_ACC	I	10 kΩ	V_{NOR}	–				
5	NC	–	–	–	–				Not connected
6	DGND	P	–	–	–				
7	VSTBY	I	–	$V_{i.MX35}$	T9		Slow	Nom	
8	WDOG_RST#	I	10 kΩ	$V_{i.MX35}$	Y12	100 kΩ	Slow	Nom	
9	PWM	O	–	$V_{i.MX35}$	Y11	Keeper	Slow	Nom	
10	JTAG_RESET#	I	10 kΩ	V_{DRV}	(U10)				
11	DGND	P	–	–	–				
12	RESET_IN#	I	10 kΩ	V_{DRV}	(U10)				
13	SSI_TXD	I/O	–	$V_{i.MX35}$	M2	100 kΩ	Slow	Nom	
14	POR#	O	10 kΩ	V_{POR}	(W11)				
15	SSI_RXD	I/O	–	$V_{i.MX35}$	L1	100 kΩ	Slow	Nom	
16	DGND	P	–	–	–				
17	SSI_TXC	I/O	–	$V_{i.MX35}$	L4	100 kΩ	Slow	Nom	
18	LD0	O	–	$V_{i.MX35}$	F20	100 kΩ	Fast	Nom	
19	SSI_TXFS	I/O	–	$V_{i.MX35}$	L2	100 kΩ	Slow	Nom	
20	LD1	O	–	$V_{i.MX35}$	G18	100 kΩ	Fast	Nom	
21	DGND	P	–	–	–				
22	LD2	O	–	$V_{i.MX35}$	G17	100 kΩ	Fast	Nom	
23	LD3	O	–	$V_{i.MX35}$	G16	100 kΩ	Fast	Nom	
24	LD4	O	–	$V_{i.MX35}$	G19	100 kΩ	Fast	Nom	
25	LD5	O	–	$V_{i.MX35}$	H16	100 kΩ	Fast	Nom	
26	DGND	P	–	–	–				
27	LD7	O	–	$V_{i.MX35}$	G20	100 kΩ	Fast	Nom	
28	LD6	O	–	$V_{i.MX35}$	H18	100 kΩ	Fast	Nom	
29	LD9	O	–	$V_{i.MX35}$	H19	100 kΩ	Fast	Nom	
30	LD8	O	–	$V_{i.MX35}$	H17	100 kΩ	Fast	Nom	
31	DGND	P	–	–	–				

Table 9: Pin description X2 (continued)

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
32	LD10	O	–	$V_{i.MX35}$	H20	100 kΩ	Fast	Nom	
33	LD11	O	–	$V_{i.MX35}$	J18	100 kΩ	Fast	Nom	
34	LD12	O	–	$V_{i.MX35}$	J16	100 kΩ	Fast	Nom	
35	LD13	O	–	$V_{i.MX35}$	J19	100 kΩ	Fast	Nom	
36	DGND	P	–	–	–				
37	LD15	O	–	$V_{i.MX35}$	J20	100 kΩ	Fast	Nom	
38	LD14	O	–	$V_{i.MX35}$	J17	100 kΩ	Fast	Nom	
39	LD17	O	–	$V_{i.MX35}$	K19	100 kΩ	Fast	Nom	
40	LD16	O	–	$V_{i.MX35}$	K14	100 kΩ	Fast	Nom	
41	DGND	P	–	–	–				
42	LD18	O	–	$V_{i.MX35}$	K18	100 kΩ	Fast	Nom	
43	LD19	O	–	$V_{i.MX35}$	K20	100 kΩ	Fast	Nom	
44	LD20	O	–	$V_{i.MX35}$	K16	100 kΩ	Fast	Nom	
45	LD21	O	–	$V_{i.MX35}$	K17	100 kΩ	Fast	Nom	
46	DGND	P	–	–	–				
47	LD23	O	–	$V_{i.MX35}$	L19	100 kΩ	Fast	Nom	
48	LD22	O	–	$V_{i.MX35}$	K15	100 kΩ	Fast	Nom	
49	LD_DRDY	O	–	$V_{i.MX35}$	L20		Fast	Nom	
50	LD_SPL	O	–	$V_{i.MX35}$	M18		Fast	Nom	
51	DGND	P	–	–	–				
52	LD_REV	O	–	$V_{i.MX35}$	M17		Fast	Nom	
53	LD_HSYNC	O	–	$V_{i.MX35}$	L18		Fast	Nom	
54	LD_CLS	O	–	$V_{i.MX35}$	L17		Fast	Nom	
55	LD_VSYNC	O	–	$V_{i.MX35}$	M19		Fast	Nom	
56	DGND	P	–	–	–				
57	DGND	P	–	–	–				
58	LD_CONTRAST	O	–	$V_{i.MX35}$	L16		Fast	Nom	
59	LD_CLK	O	–	$V_{i.MX35}$	L15		Fast	Nom	
60	USBHS_OC	I	–	V_{USB}	–				
61	DGND	P	–	–	–				
62	USBHS_PSW#	O	100 kΩ	V_{USB}	–				

Table 9: Pin description X2 (continued)

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
63	USBHS_UID	I	0 Ω	V_{USB}	–				Configured as Host
64	USBHS_VBUS	I/O	100 kΩ	V_{USB}	–				
65	DGND	P	–	–	–				
66	DGND	P	–	–	–				
67	USBHS_UDP	I/O	–	V_{USB}	–		–	–	
68	USB_OTG_OC	I	–	V_{USB}	U7	100 kΩ	Slow	Nom	
69	USBHS_UDM	I/O	–	V_{USB}	–		–	–	
70	USB_OTG_PWR	O	–	V_{USB}	W7		Slow	Nom	
71	DGND	P	–	–	–				
72	USB_OTG_UID	I	–	V_{USB}	N18	–	–	Nom	
73	USB_OTG_DM	I/O	–	V_{USB}	N19	–	–	Nom	
74	USB_OTG_VBUS	I/O	–	V_{USB}	P18	–	–	Nom	
75	USB_OTG_DP	I/O	–	V_{USB}	P19	–	–	Nom	
76	DGND	P	–	–	–				
77	DGND	P	–	–	–				
78	SD1_DAT0	I/O	–	$V_{i.MX35}$	R14	47 kΩ	Fast	High	
79	SD1_CLK	O	–	$V_{i.MX35}$	V18	47 kΩ	Fast	High	
80	SD1_DAT1	I/O	–	$V_{i.MX35}$	U16	47 kΩ	Fast	High	
81	DGND	P	–	–	–				
82	SD1_DAT2	I/O	–	$V_{i.MX35}$	W18	47 kΩ	Fast	High	
83	SD1_CMD	I/O	–	$V_{i.MX35}$	Y19	47 kΩ	Fast	High	
84	SD1_DAT3	I/O	–	$V_{i.MX35}$	V17	100 kΩ	Fast	High	
85	CSI_D1	I	–	$V_{i.MX35}$	R3		Slow	Nom	
86	DGND	P	–	–	–				
87	CSI_D3	I	–	$V_{i.MX35}$	T5		Slow	Nom	
88	CSI_D0	I	–	$V_{i.MX35}$	U1	100 kΩ	Slow	Nom	
89	CSI_D5	I	–	$V_{i.MX35}$	R4		Slow	Nom	
90	CSI_D2	I	–	$V_{i.MX35}$	V2	100 kΩ	Slow	Nom	
91	DGND	P	–	–	–				
92	CSI_D4	I	–	$V_{i.MX35}$	T3	100 kΩ	Slow	Nom	
93	CSI_D7	I	–	$V_{i.MX35}$	R5		Slow	Nom	
94	CSI_D6	I	–	$V_{i.MX35}$	V1		Slow	Nom	

Table 9: Pin description X2 (continued)

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
95	CSI_D9	I	10 kΩ	$V_{i.MX35}$	W17	Keeper	Fast	Nom	
96	DGND	P	–	–	–				
97	CSI_D11	I	10 kΩ	$V_{i.MX35}$	T15	Keeper	Fast	Nom	
98	CSI_D8	I	10 kΩ	$V_{i.MX35}$	U15	Keeper	Fast	Nom	
99	CSI_D13	I	10 kΩ	$V_{i.MX35}$	V15	Keeper	Fast	Nom	
100	CSI_D10	I	10 kΩ	$V_{i.MX35}$	V16	Keeper	Fast	Nom	
101	DGND	P	–	–	–				
102	CSI_D12	I	10 kΩ	$V_{i.MX35}$	W16	Keeper	Fast	Nom	
103	CSI_D15	I	1 kΩ	$V_{i.MX35}$	Y16	Keeper	Fast	Nom	
104	CSI_D14	I	10 kΩ	$V_{i.MX35}$	U14	Keeper	Fast	Nom	
105	CSI_VSYNC	I	10 kΩ	$V_{i.MX35}$	T14	Keeper	Fast	Nom	
106	DGND	P	–	–	–				
107	CSI_HSYNC	I	10 kΩ	$V_{i.MX35}$	V14	Keeper	Fast	Nom	
108	CSI_MCLK	O	–	$V_{i.MX35}$	W15		Fast	Nom	
109	CSI_PIXCLK	I	–	$V_{i.MX35}$	Y15	Keeper	Fast	Nom	
110	DE#	I/O	–	$V_{i.MX35}$	W19	100 kΩ	Slow	Nom	
111	DGND	P	–	–	–				
112	RTCK	O	1 kΩ	$V_{i.MX35}$	U18	100 kΩ	Fast	High	
113	TCK	I	1 kΩ	$V_{i.MX35}$	R17	100 kΩ	Slow	Nom	
114	JTAG_MOD	I	1 kΩ	$V_{i.MX35}$	U17	100 kΩ	Slow	Nom	
115	TMS	I	10 kΩ	$V_{i.MX35}$	R16	100 kΩ	Slow	Nom	
116	DGND	P	–	–	–				
117	TDI	I	10 kΩ	$V_{i.MX35}$	P15	100 kΩ	Slow	Nom	
118	TDO	O	10 kΩ	$V_{i.MX35}$	R15	100 kΩ	Fast	High	
119	DGND	P	–	–	–				
120	TRST#	I	10 kΩ	$V_{i.MX35}$	T16	100 kΩ	Slow	Nom	

4.1.3.3 Module connector X3 [7]

Table 10: Pin description X3

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
1	DGND	P	–	–	–				
2	D0	I/O	–	$V_{i.MX35}$	A2	Keeper	Fast	High	
3	D1	I/O	–	$V_{i.MX35}$	D4	Keeper	Fast	High	
4	D2	I/O	–	$V_{i.MX35}$	B2	Keeper	Fast	High	
5	D3	I/O	–	$V_{i.MX35}$	E5	Keeper	Fast	High	
6	DGND	P	–	–	–				
7	D5	I/O	–	$V_{i.MX35}$	B1	Keeper	Fast	High	
8	D4	I/O	–	$V_{i.MX35}$	C3	Keeper	Fast	High	
9	D7	I/O	–	$V_{i.MX35}$	C2	Keeper	Fast	High	
10	D6	I/O	–	$V_{i.MX35}$	D3	Keeper	Fast	High	
11	DGND	P	–	–	–				
12	D8	I/O	–	$V_{i.MX35}$	C1	Keeper	Fast	High	
13	D9	I/O	–	$V_{i.MX35}$	E4	Keeper	Fast	High	
14	D10	I/O	–	$V_{i.MX35}$	D2	Keeper	Fast	High	
15	D11	I/O	–	$V_{i.MX35}$	E6	Keeper	Fast	High	
16	DGND	P	–	–	–				
17	D13	I/O	–	$V_{i.MX35}$	F5	Keeper	Fast	High	
18	D12	I/O	–	$V_{i.MX35}$	E3	Keeper	Fast	High	
19	D15	I/O	–	$V_{i.MX35}$	E2	Keeper	Fast	High	
20	D14	I/O	–	$V_{i.MX35}$	D1	Keeper	Fast	High	
21	DGND	P	–	–	–				
22	ADDR0	O	–	V_{BUF}	(A5)				
23	ADDR1	O	–	V_{BUF}	(D7)				
24	ADDR2	O	–	V_{BUF}	(E7)				
25	ADDR3	O	–	V_{BUF}	(C6)				
26	DGND	P	–	–	–				
27	ADDR5	O	–	V_{BUF}	(B5)				

[7] Depends on placement option.

Table 10: Pin description X3 (continued)

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
28	ADDR4	O	–	V_{BUF}	(D6)				
29	ADDR7	O		V_{BUF}	(A4)				
30	ADDR6	O	–	V_{BUF}	(C5)				
31	DGND	P	–	–	–				
32	ADDR8	O	–	V_{BUF}	(B4)				
33	ADDR9	O	–	V_{BUF}	(A3)				
34	ADDR10	O	–	V_{BUF}	(F15)				
35	ADDR11	O	–	V_{BUF}	(D5)				
36	DGND	P	–	–	–				
37	ADDR13	O	–	V_{BUF}	(B3)				
38	ADDR12	O	–	V_{BUF}	(F6)				
39	ADDR15	O	–	V_{BUF}	(D15)				
40	ADDR14	O	–	V_{BUF}	(D14)				
41	DGND	P	–	–	–				
42	ADDR16	O	–	V_{BUF}	(D13)				
43	ADDR17	O	–	V_{BUF}	(C13)				
44	ADDR18	O	–	V_{BUF}	(D12)				
45	ADDR19	O	–	V_{BUF}	(D11)				
46	DGND	P	–	–	–				
47	ADDR21	O	–	V_{BUF}	(D10)				
48	ADDR20	O	–	V_{BUF}	(C10)				
49	ADDR23	O	–	V_{BUF}	(C7)				
50	ADDR22	O	–	V_{BUF}	(D9)				
51	DGND	P	–	–	–				
52	ADDR24	O	–	V_{BUF}	(D8)				
53	ADDR25	O	–	V_{BUF}	(E8)				
54	LBA#	O	–	V_{BUF}	(D20)				
55	DTACK#	I	–	V_{BUF}	(E18)				
56	DGND	P	–	–	–				
57	DGND	P	–	–	–				
58	RW#	O	–	V_{BUF}	(C20)				

Table 10: Pin description X3 (continued)

Pin	Pin name	Direction	External pull-up / -down	VCCIO	i.MX35 Parameter				Remark
					CPU-Pin	Internal pull / Keeper	Slew rate	Drive strength	
59	BUS_CLK	O	–	V_{BUF}	(E15)				
60	OE#	O	–	V_{BUF}	(E20)				
61	DGND	P	–	–	–				
62	ECB#	I	10 kΩ	V_{BUF}	(D19)				
63	EB1#	O	–	V_{BUF}	(F16)				
64	EB0#	O	–	V_{BUF}	(F18)				
65	CS1#	O	–	V_{BUF}	(E19)				
66	DGND	P	–	–	–				
67	CS5#	O	–	V_{BUF}	(F19)				
68	DNC	–	–	–	–				Do not connect
69	DNC	–	–	–	–				Do not connect
70	DNC	–	–	–	–				Do not connect
71	DGND	P	–	–	–				
72	DNC	–	–	–	–				Do not connect
73	DNC	–	–	–	–				Do not connect
74	DNC	–	–	–	–				Do not connect
75	DNC	–	–	–	–				Do not connect
76	DGND	P	–	–	–				
77	DNC	–	–	–	–				Do not connect
78	NC	–	–	–	–				Not connected
79	DGND	P	–	–	–				
80	NC	–	–	–	–				Not connected

4.1.4 Electrical characteristics

Table 11: Electrical characteristics of digital I/Os

Parameter	Min.	Typ.	Max.	Unit	Remark
$V_{i.MX35}$					
Output voltage High-level V_{OH}	0.8 × VIN			V	Drive strength nominal, high resp. max.
Output voltage Low-level V_{OL}			0.2 × VIN	V	Drive strength nominal, high resp. max.
Output current High-level I_{OH} (slew rate: slow, V_{OH} = 0.8 × VIN)	–2.0 –4.0 –8.0			mA	Nominal drive High drive Max drive
Output current High-level I_{OH} (slew rate: fast, V_{OH} = 0.8 × VIN)	–4.0 –6.0 –8.0			mA	Nominal drive High drive Max drive
Output current Low-level I_{OL} (slew rate: slow, V_{OL} = 0.2 × VIN)	2.0 4.0 8.0			mA	Nominal drive High drive Max drive
Output current Low-level I_{OL} (slew rate: fast, V_{OL} = 0.2 × VIN)	4.0 6.0 8.0			mA	Nominal drive High drive Max drive
Input voltage High-level V_{IH}	0.7 × VIN		VIN	V	
Input voltage Low-level V_{IL}	–0.3		0.3 × VIN	V	
V_{BUF}					
Output voltage High-level V_{OH}	2.4		VIN	V	I_{OH} = –12 mA
Output voltage Low-level V_{OL}			0.8	V	I_{OL} = 12 mA
Output current High-level I_{OH}	–12			mA	
Output current Low-level I_{OL}	12			mA	
Input voltage High-level V_{IH}	2.0		3.6	V	
Input voltage Low-level V_{IL}			0.8	V	
V_{DRV}					
Input voltage High-level V_{IH}	2.0		5.5	V	
Input voltage Low-level V_{IL}			0.8	V	
V_{POR}					
Output voltage Low-level V_{OL} (open drain)			0.3	V	I_{SINK} = 1.2 mA
V_{NOR}					
Input voltage High-level V_{IH}	0.7 × VIN		VIN + 0.4	V	
Input voltage Low-level V_{IL}	–0.5		0.8	V	

Table 12: Electrical characteristics of the physical signals

Parameter	Description
V_{USB}	
Type of media	USB 2.0 Hi-Speed Host OTG
Interface module	USB Host resp. OTG physical
Signal characteristic	Compatible to Universal Serial Bus specification Rev. 2.0
ESD protection	±2 kV Human Body Model
V_{RS232} [8]	
Transfer rate	Up to 120 Kbit/s
Interface CPU	UART1
Handshake	None
Signal characteristic	Compatible to EIA/TIA-232 standard
ESD protection	±15 kV Human Body Model

4.2 User's interfaces

On the TQMa35, a red LED indicates the reset condition.

Table 13: State of the Reset-LED

State LED	Level POR#	Description
ON	Low	Module is in Reset
OFF	High	Normal operation

4.3 System components

4.3.1 Processor

The Freescale processor i.MX35 (MCIMX35) based on the ARM1136JF-S™ core is manufactured in 90 nm technology. It provides a wide range of functions. Illustration 2 gives an overview.
The CPU is available in two revisions (Tape-Outs). On the TQMa35 Rev. 2.1 is used, because the SDRAM interface in Rev. 2.0 can cause errors. Additional termination must be provided for some control signals of Rev. 2.0.
Depending on placement option, one of the two pin-compatible derivatives i.MX353 and i.MX357 is used. The i.MX357 contains an additional OpenVG 1.1 hardware acceleration for 2D vector and bit-mapped graphics.
In the following table the i.MX35 CPUs of Rev. 2.1 are listed.

[8] Depends on placement option (UART1 used as RS232).

Table 14: Processor derivatives

Manufacturer	Part number	Temperature range	Housing	Silicon revision
Freescale	MCIMX353**D**JQ5C	–20 to +85 °C	BGA400	2.1
Freescale	MCIMX357**D**JQ5C	–20 to +85 °C	BGA400	2.1
Freescale	MCIMX353**C**JQ5C	–40 to +85 °C	BGA400	2.1
Freescale	MCIMX357**C**JQ5C	–40 to +85 °C	BGA400	2.1

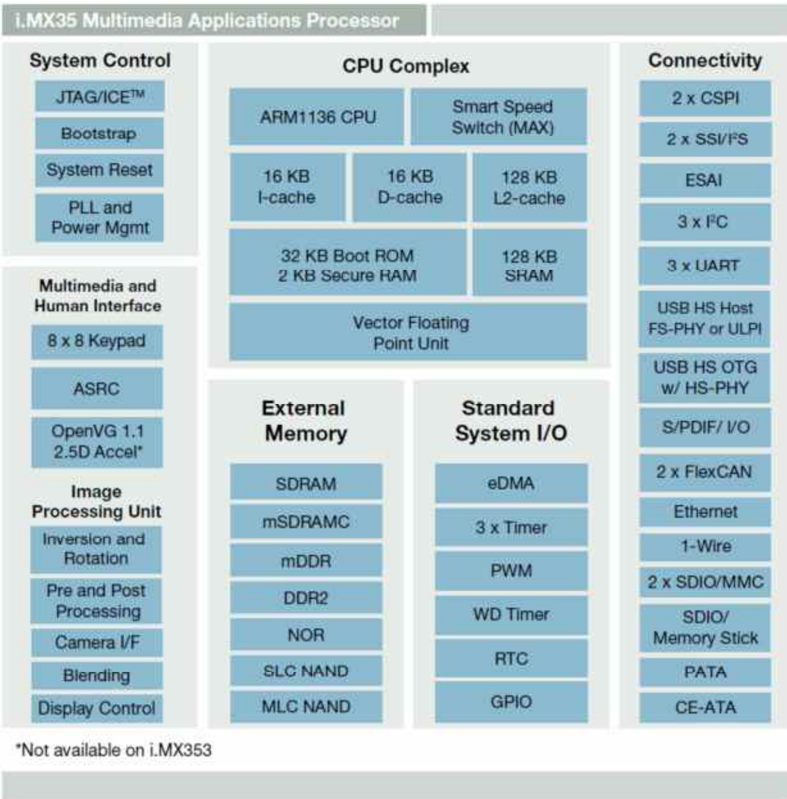


Illustration 2: i.MX35 block diagram
(Source: Freescale)

Key functionalities

ARM1136 CPU:

- I-Cache, D-Cache, L2-Cache
- Integrated SRAM
- Jazelle Java Acceleration
- VFP – Vector Floating Point Co-processor (only i.MX357)
- CPU clock: 532 MHz

ESDRAMC – enhanced synchronous dynamic RAM controller:

- SDRAM 16/32 bit / (m)DDR 16/32 bit
- DDR2 (limited support)

WEIM – Wireless External Interface Module:

- NOR Flash
- NAND Flash
- PSRAM (CellularRAM™)

Multimedia:

- IPU - Image Processing Unit
- CMOS/CCD Sensor Interface
- LCD Controller (up to 24-bit-per-pixel WVGA)

Interfaces:

- USB OTG High Speed (host and device)
- PATA/CE-ATA
- 2 × FlexCAN modules
- Configurable SPI × 2, SSI/I2S × 2, UART × 3, MMC/SDIO, I^{2}C × 3

Package:

- Temperature range: –40 °C to +85 °C, BGA-400, 0.8 mm grid
- Temperature range: –20 °C to +70 °C, BGA-400, 0.8 mm grid

Further functionality of the processor shown in the block diagram can be looked up in the Reference Manual.
All essential pins of the processor, except the DDR-SDRAM interface, are routed to the module connectors.

4.3.1.1 Boot modes

The boot mode of the i.MX35 is configured by default in a boot sequence after the reset, by reading the voltage levels of the dedicated boot mode pins. The following table shows the relevant pins as well as the assignment of the matching resistors for the TQMa35.

Table 15: Configurable boot pins on the TQMa35

Pin	Name	eFuse-name	Function	Configuration resistors	
				Pull-up	Pull-down
W10	BOOT_MODE0	–	Boot mode select pins	R47	R49
U9	BOOT_MODE1	–		R46	R48
U15	CSI_D8	BT_MEM_CTL[0]	Boot memory device	R53	R52
W17	CSI_D9	BT_MEM_CTL[1]		R54	R55
V16	CSI_D10	BT_MEM_TYPE[0]	Boot memory type	R59	R58
T15	CSI_D11	BT_MEM_TYPE[1]		R56	R57
W16	CSI_D12	BT_PAGE_SIZE[0]	NAND Flash page size	R67	R66
V15	CSI_D13	BT_PAGE_SIZE[1]		R64	R65
U14	CSI_D14	BT_ECC_SEL	Define 4/8-bit ECC	R63	R62
Y16	CSI_D15	BT_USB_SRC[0]	USB PHY selection	R60	R61
V14	CSI_HSYNC	BT_USB_SRC[1]		R51	R50
T14	CSI_VSYNC	BT_BUS_WIDTH	NAND bus width	R44	R45

As shown in Table 16 different modes can be configured on the TQMa35.
Pre-configured standard boot-mode is “NOR flash (WEIM bus)”.
To boot from e.g. an SD card or eMMC flash, the configuration of the resistors on the module has to be changed.
Table 16 shows the configurations possible on the TQMa35.
Should the module be booted from the SD3 interface instead of the SD1 interface, the eFuse BT_SDMMC_SRC[1] must be burnt.
Therefore Fuse_VDD must be connected to 3.3 V during the writing process.

Table 16: Possible boot mode configurations for the TQMa35

Boot pins									Boot mode
BOOT_MODE0	BOOT_MODE1	CSI_D8	CSI_D9	CSI_D10	CSI_D11	CSI_D15	CSI_HSYNC	CSI_VSYNC	
0	0	0	0	0	0	x	x	0	Internal Boot mode, NOR flash
0	0	1	1	0	0	x	x	x	Internal Boot mode, SD card 1
0	0	1	1	0	1	x	x	x	Internal Boot mode, serial ROM via I²C1
0	0	1	1	1	1	x	x	0	Internal Boot mode, serial ROM via SPI1 (2 byte address)
0	0	1	1	1	1	x	x	1	Internal Boot mode, serial ROM via SPI1 (3 byte address)
0	**1**	**0**	**0**	**0**	**0**	**x**	**x**	**0**	**External (direct) Boot mode, NOR flash (default)**
1	1	x	x	x	x	x	x	x	Serial boot loader, UART1
1	1	x	x	x	x	0	0	x	Serial boot loader, UTMI PHY
1	1	x	x	x	x	1	0	x	Serial boot loader, ULPI PHY

4.3.1.2 Memory management

Different types of memory, which share the address bus, are assembled on the TQMa35.
On a carrier board additional devices can also be addressed.
The memory allocation of the TQMa35 is shown in the following table.

Table 17: External Memory allocation

Address range	Chip select	Function
0xA000 0000 ... 0xA7FF FFFF	CS0#	NOR flash (max. 128 MiB)
0xA800 0000 ... 0xAFFF FFFF	CS1#	Module connector X3 (max. 128 MiB)
0x8000 0000 ... 0x8FFF FFFF	CSD0#	mDDR SDRAM (max. 256 MiB)
0x9000 0000 ... 0x9FFF FFFF	CSD1#	mDDR SDRAM (max. 256 MiB)
0xB400 0000 ... 0xB5FF FFFF	CS4# / DTACK# [9]	Module connector X3 (max. 32 MiB)
0xB600 0000 ... 0xB7FF FFFF	CS5#	Module connector X3 (max. 32 MiB)

4.3.1.3 Pin multiplexing

Depending on the configuration, the pin multiplexing enables different pins to have different functions.

Attention: Destruction or malfunction!



Many of the CPU pins can be used in several different ways.
Please, notice the notes about the wiring of these pins in the Reference Manual of the i.MX35 before integration / start-up of your carrier board / Starterkit.

4.3.1.4 CPU-Errata

Attention: Malfunction!



Please pay attention to the current errata of the Freescale CPU.

[9] Fixed configured as DTACK# signal, CS4# cannot be used.

4.3.2 Memory

4.3.2.1 mDDR SDRAM

The module can be equipped with 128 MiB, 256 MiB or 512 MiB.
For the size of 128 MiB only one memory device is required.
For 256 MiB as well as 512 MiB two devices are required.
Two 32-bit wide RAM chips work parallel at the chip selects CSD0# and CSD1# in the maximum expansion stage (512 MiB). Both chips selects can address up to 256 MiB.
Both memory chips share all signals except chip select and clock enable signals.
The memory controller of the i.MX35 supports clock frequencies of up to 133 MHz.
Table 18 gives an overview of the possible alternatives.
As a standard component placement the memory of Hynix is assembled.

Table 18: Memory models mDDR SDRAM

Manu-facturer	128 MiB		256 MiB	
	Part Number	Temperature	Part Number	Temperature
Hynix	H5MS1G22MFP-J3M	–30 to +85 °C	H5MS2G22MFR-J3M	–30 to +85 °C
Micron	MT46H32M32LFCM-6 IT	–40 to +85 °C	MT46H64M32LFCM-6 IT	–40 to +85 °C

Attention: Temperature range

Only Micron offers mDDR memory for the temperature range of –40 to +85 °C.
The temperature range of the module is limited to –30 to +85 °C respective –25 to +85 °C when the alternative memory is used.

4.3.2.2 NOR flash

The module can be assembled with 32 MiB, 64 MiB or 128 MiB of NOR flash.
The functions WP# and RST# can be controlled directly via the carrier board when required.
Defined states are configured on the module for both signals.
In the following table the version is shown, which can be assembled.

Table 19: Memory model NOR flash

Manufacturer	32 MiB	64 MiB	128 MiB
Numonyx	PC28F256M29EWL	PC28F512M29EWL	PC28F00AM29EWL

In the version with WEIM bus all signals of the NOR flash (except BYTE#) are additionally available directly at the module connector.

4.3.2.3 eMMC

Depending on the version of the TQMa35 an eMMC-Flash is assembled.
It is controlled by one of the SD card controllers of the i.MX35.
The processor has an SD host interface according to specification 4.2.
To be able to use the interface with not equipped eMMC flash, the signals are additionally routed to the module connector via short branch lines.

Table 20: Memory model eMMC flash

Manufacturer	2 GiB		
	Part number	MMCA Rev.	Temperature
Toshiba	THGBM1G4D1EBAI7DTH	4.3	–25 °C to +85 °C

Attention: Use of SD3 interface
The SD3 bus is available on the module connectors. It may however only be used, if the eMMC flash is not equipped.

Attention: Temperature range
Only Micron offers eMMC memory for the temperature range of –40 to +85 °C. When using the Toshiba memory the temperature range of the module is limited to –25 to +85 °C.

4.3.2.4 EEPROM

Depending on the assembly option a serial 64 Kibit EEPROM is available for permanent storage of e.g. module characteristics or customers parameters. The EEPROM is controlled via I²C bus 2 of the processor. An EEPROM with a size of 64 Kibit is assembled by default. Detailed information concerning the I²C-address configuration can be found in section 4.3.10.4. The write protection (WP) of the EEPROM is not available.

Table 21: Memory model EEPROM

Manufacturer	Part number
ST Microelectronics	M24C64-WDW6TP

4.3.3 WEIM bus [10]

Depending on the assembly option the 16-bit-wide, external interface is available at the additional module connector X3. All 26 address signals as well as all usable control signals are routed via line drivers to raise the I/O voltage from 1.8 V to V_{IN}. The chip selects CS0#, CS2#, CS3# and CS4# are not available. For more information see Table 17 on page 33.

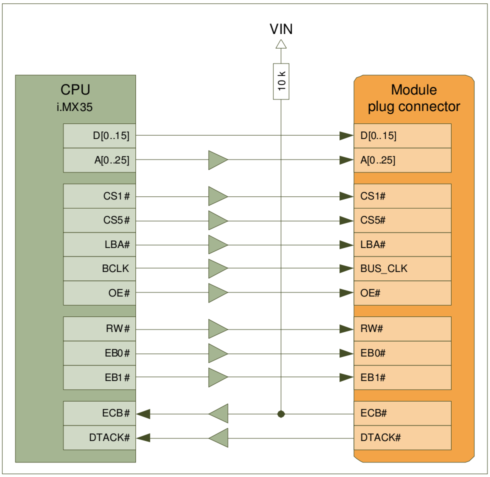


Illustration 3: Interface WEIM bus

The pull-up resistor at ECB# is only assembled on versions with NOR-Flash.

[10] Depends on placement option.

4.3.4 RTC

On the TQMa35 an RTC (Dallas DS1339U-33+) is available. The connection of the RTC is shown in section 4.3.10.4. The output SQW/INT# of the RTC is available at the module connector, as well as at the processor (pin J2) as a placement option. A 32.768 kHz crystal oscillator clocks the RTC. The parameters of the crystal oscillator are shown in the following table.

Table 22: Parameter 32.768 kHz crystal oscillator

Parameter	Value	Unit	Remark
Frequency tolerance versus temperature	±20	ppm	25 °C
	±50	ppm	–40 to +85 °C
Frequency ageing	±3 max.	ppm	per year, @ 25 °C

It is possible to buffer the RTC via the module connector with a battery. When power is switched off the RTC circuit automatically switches to the backup supply. For more information regarding buffering the RTC see paragraph 4.3.18 on page 48.

4.3.5 Temperature sensor

A National Semiconductor LM75 temperature sensor is present. The sensor is placed on the bottom side of the module (see D15 in Illustration 20). The connection of the sensor is shown in section 4.3.10.4.
The “OS”-output (over-temperature shutdown) of the sensor including a 10 kΩ pull-up at the processor (pin G3) is optionally available at the module connector.

4.3.6 SD card

The TQMa35 offers two SD card controllers, which are available at the module connectors. The first controller (SD1) is always available, the second controller (SD3) cannot be used on module versions with eMMC flash.

Table 23: Transfer modes SD interfaces

CPU interface	Supported data transfer modes		
	One-Bit	Four-Bit	Eight-Bit
SD1	Yes	Yes	No
SD3	Yes	Yes	Yes

Attention: Use of the SD interface
The pull-up resistors, which are required for the operation of the SD interfaces, must be implemented on the carrier board.

4.3.7 Graphics interfaces

4.3.7.1 LCD bus

Parallel displays with a maximum frame size of up to 1024 × 1024 pixels can be connected to the TQMa35. The parallel data interface can be up to 24 bits wide.
To connect an LCD the display 3 interface of the CPU is used.
The LCD bus is directly routed to the module connector.

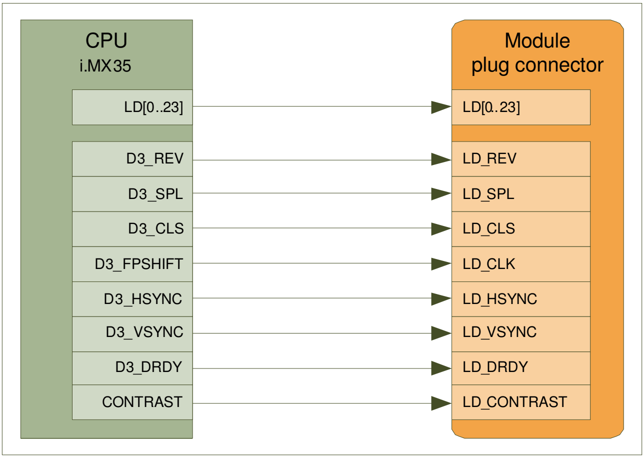


Illustration 4: Interface LCD

4.3.7.2 Sensor interface

Sensor data can be fed directly via the module connectors to the "Camera Sensor Interface" of the i.MX35 (see Illustration 5).

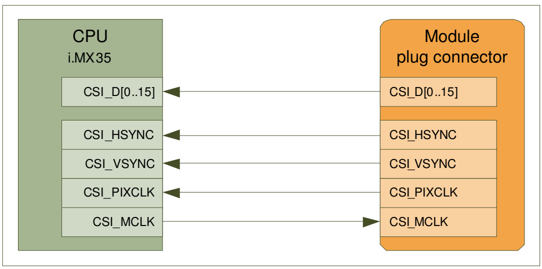


Illustration 5: Interface CSI

4.3.8 USB Hi-Speed

4.3.8.1 USB On-The-Go

The CPU-internal transceiver of the i.MX35 is used for the USB On-The-Go interface.
The 5 V supply for the USB ports has to be implemented on the carrier board.

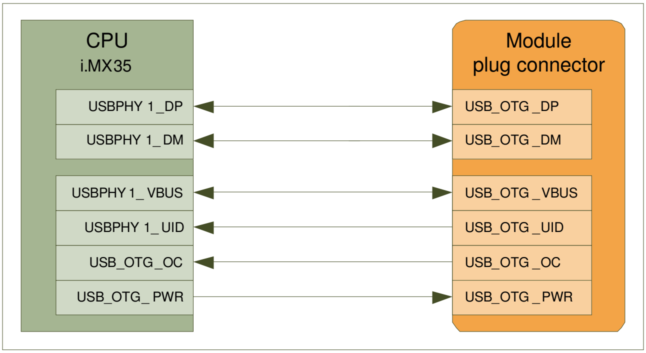


Illustration 6: Interface USB OTG

Filtering and EMC protection for the USB signals has to be provided on the carrier board. Notes are to be found in the USB standard.
For the use of the USB UTMI PHY a workaround is shown in the errata of the i.MX35
(see Illustration 7). This workaround is provided on the TQMa35. This ensures that at certain voltage levels the input impedance of VBUS does not become too low.
To achieve this, an external voltage divider reduces the voltage at the VBUS pin to 25 %.
An 8.2 V Zener diode is switched in parallel to R_1.

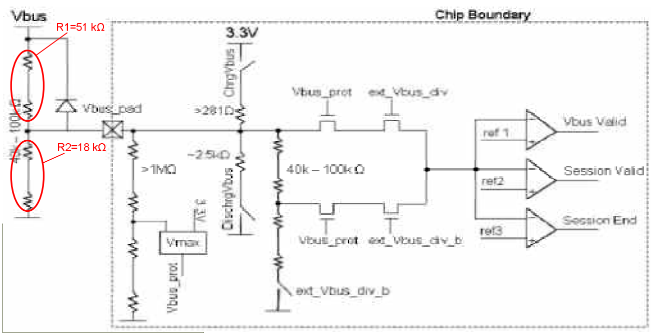


Illustration 7: USB Hi-Speed OTG workaround
(Source: IMX35CE Rev. 3)

4.3.8.2 USB Host

On the TQMa35 the USB-High-Speed-Host is implemented with an STEricsson ULPI-PHY ISP1715AETTM. The connection is displayed in the following illustration.
The 5 V supply for the USB port has to be implemented on the carrier board.
The ULPI PHY is supplied with a 26 MHz clock.

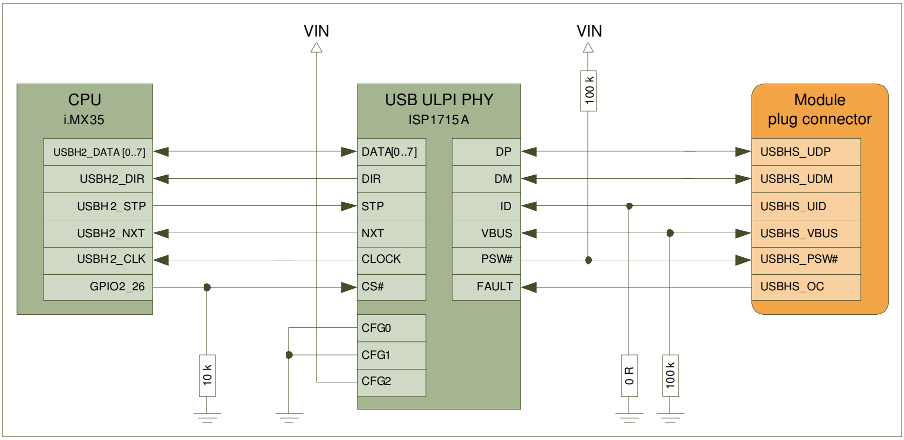


Illustration 8: Interface USB host

Filtering and EMC protection for the USB signals has to be provided on the carrier board.
Notes are to be found in the USB standard.

4.3.9 Ethernet

The i.MX35 offers a built-in Fast Ethernet controller, which is designed for 10 and 100 Mbps.
The provided MII interface is available to the user directly at the module connectors.
The Ethernet interface is completed by a PHY on the carrier board.

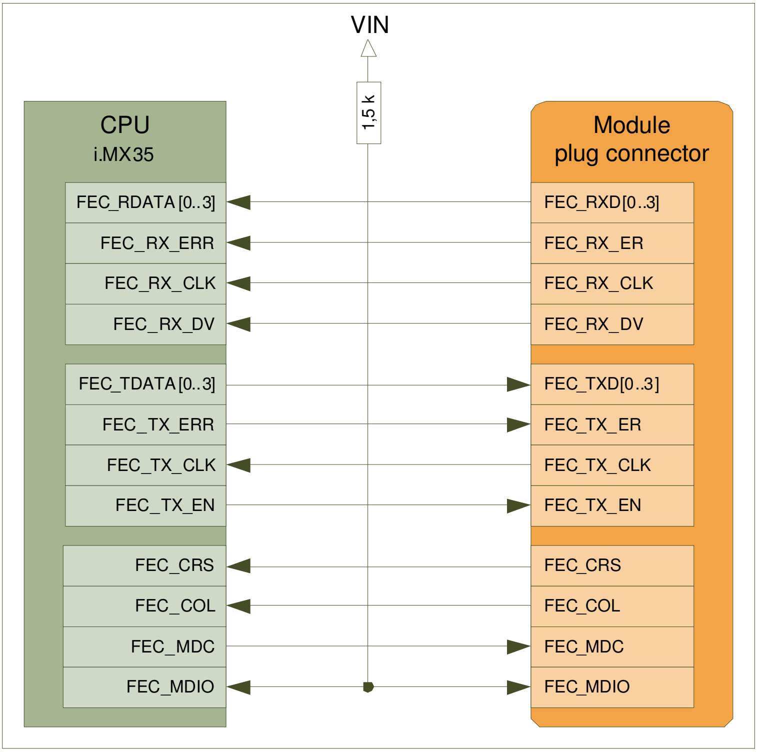


Illustration 9: Interface Ethernet MII

4.3.10 Serial interfaces

The TQMa35 provides three UART interfaces.

4.3.10.1 UART1 / RS232

To provide a communication without external hardware especially during the start-up, the voltage levels on the module are adapted by a transceiver. If the RS232 interface is not used, the signals UART1_TxD and UART1_RxD can also be routed to the module connectors as LVTTL signals. Therefore two 0 Ω resistors are provided in the layout under the RS232 driver.
These resistors can be assembled instead of the driver. The handshake signals RTS# and CTS# for the UART1 are not available, as they are used by other multiplexed signals.

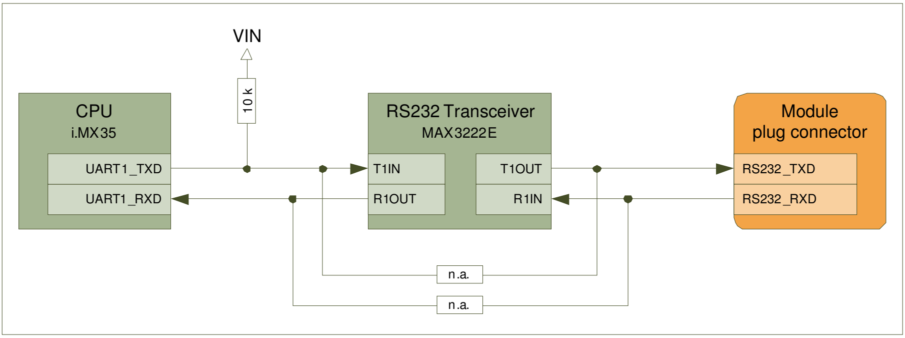


Illustration 10: Interface UART1 / RS232

4.3.10.2 UART2

The UART2 interface is available directly at the module connector.
Beside RxD and TxD the handshake signals RTS# and CTS# are also provided.

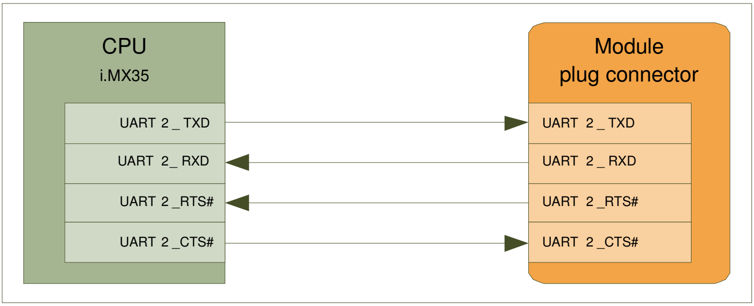


Illustration 11: Interface UART2

4.3.10.3 UART3

The UART3 interface is available directly at the module connector.
Beside RxD and TxD the handshake signals RTS# and CTS# are also provided.

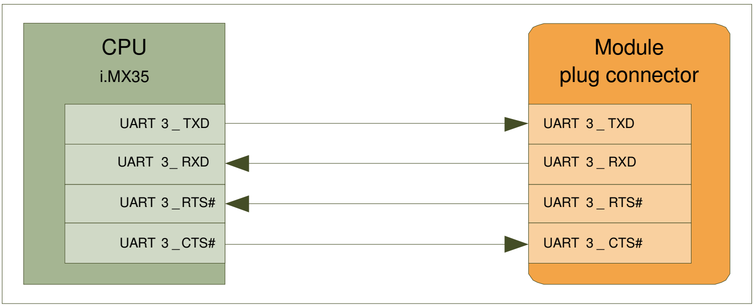


Illustration 12: Interface UART3

4.3.10.4 I²C bus

The I²C bus 1 is routed to the module connectors and not used on the TQMa35.
Three devices are connected to I²C bus 2 on the module:

- Temperature sensor
- EEPROM
- RTC

The following table shows the associated address ranges.

Table 24: I²C device configuration

Device	Device address							
	Hex	MSB	Binary					LSB
Temperature sensor	0x48	1	0	0	1	0 (A2)	0 (A1)	0 (A0)
EEPROM	0x50	1	0	1	0	0 (A2)	0 (A1)	0 (A0)
RTC	0x68	1	1	0	1	0	0	0

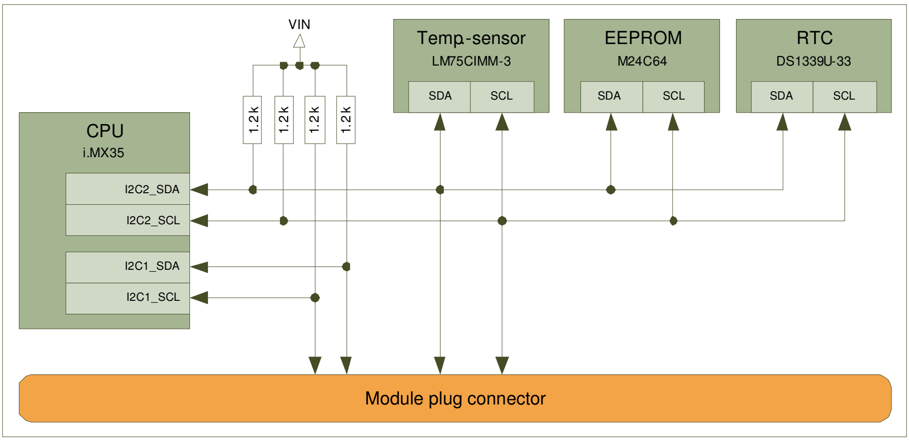


Illustration 13: Interface I²C buses

Attention: Pull-up resistors



All pull-up resistors for the I²C busses are already assembled on the module and must therefore not be equipped on the carrier board.
If more devices are connected the bus load has to be estimated.
If necessary the overall resistance has to be reduced by additional parallel resistors.

4.3.10.5 CAN

Both CPU-internal FlexCAN controllers of the i.MX35 with data rates up to 1 Mbit/s (according to CAN 2.0B protocol) are used as CAN interfaces.
The signals are routed to the module connectors.
The corresponding drivers have to be provided on the carrier board.

4.3.10.6 SPI1

Up to three devices can be connected to the SPI-1 bus.
Chip selects SS0, SS1 and SS3 are used for addressing.
SS2 however is not available in the standard BSP.
It is routed to the module connector in another multiplexed function.

4.3.10.7 SPI2

One device can be connected to the SPI-2 bus. Chip-Select SS0 is used for addressing.
SS1 to SS3 are however not available in the standard BSP.
They are routed to the module connector in other multiplexed functions.

4.3.10.8 SSI

Synchronous modes with a common clock and sync signal for transmitter and receiver can be implemented via the available 4 pin SSI4 of the i.MX35. The clock and sync signals for the implementation of asynchronous modes are used by the CAN2 interface.

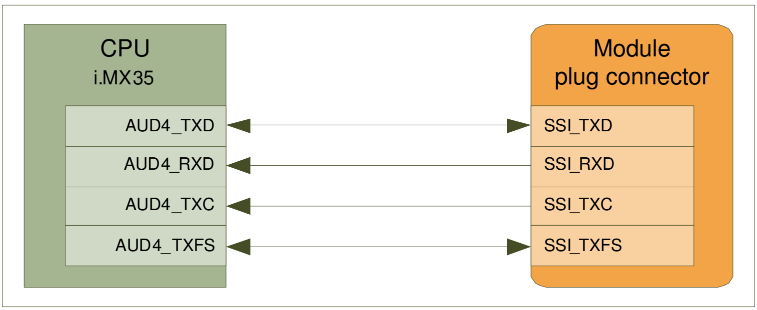


Illustration 14: Interface SSI

4.3.10.9 1-Wire

The 1-Wire interface of the i.MX35 is directly routed to a module connector.

4.3.11 PWM

The PWM output of the i.MX35 is directly accessible at a module connector pin.

4.3.12 Keypad

In the standard BSP the TQMa35 supports 16 keys in a 4×4 matrix. Therefore four of the eight ROW- or COL signals are available at a module connector.

4.3.13 GPIO

The i.MX35 processor offers GPIO ports as a second or multiple configurations with other function units. The configuration can be taken from the Freescale Reference Manual.
Some of the GPIOs are directly named as GPIO and routed directly to the module connector.
All GPIOs are interrupt and wakeup-capable.
A sequence for a wakeup, triggered by a GPIO interrupt, is displayed in the following illustration.

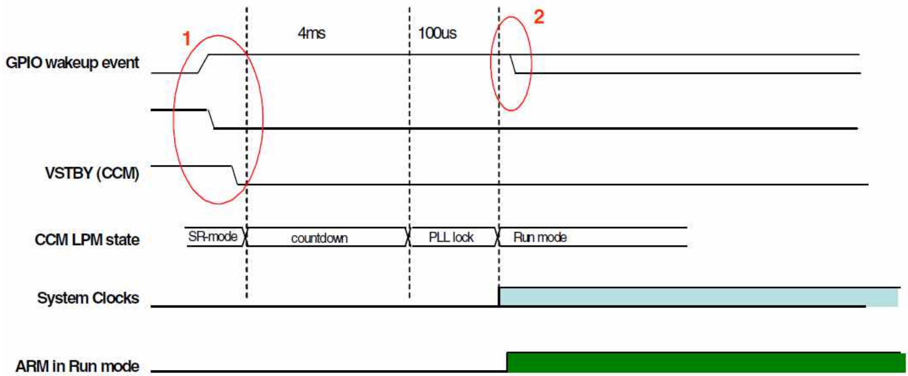


Illustration 15: Timing diagram of a GPIO wakeup interrupt
(Source: i.MX35 Reference Manual Rev. 3)

4.3.14 Timer

One capture and one compare channel of the CPU's general purpose timer is available at the module connector.

4.3.15 BDM/JTAG

The BDM/JTAG signals are directly routed from the CPU to the module connector.
All necessary pull-up and pull-down resistors are present on the TQMa35.

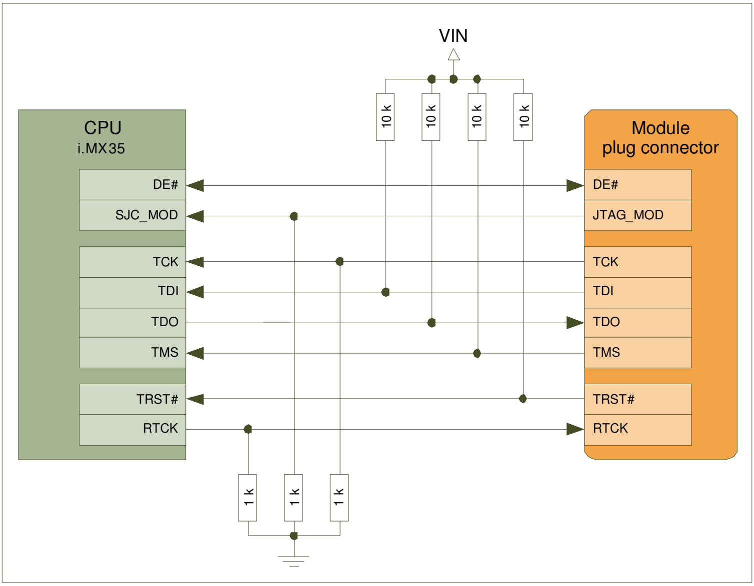


Illustration 16: Interface BDM/JTAG

4.3.16 Power management

The TQMa35 works with a supply voltage of 3.3 V (±4 %) that must be provided by the carrier board.
In the following table the data of the supply voltage is shown. The calculated current consumption (worst case) is at most 0.8 A. In average the current consumption will be approximately 0.2 to 0.4 A. The current consumption strongly depends on component placement, software and wiring options.

Table 25: Technical parameters module supply

Parameter	Min.	Typ.	Max.	Unit	Remark
Supply voltage V_{IN}	3.17	**3.3**	3.43	V	V_{IN} is limited by the electrical parameters of the i.MX35 (analog voltage of the USB PHY1)
Current consumption		0.28	0.8	A	Value depends i.e. on the size of memory
Current consumption (Idle Mode)		0.14		A	For more information see (11)
Current consumption (Standby)		20		mA	For more information see (11)

4.3.17 Voltage supervision

The switching regulators work down to a voltage of 2.8 V. A supervisor is used which monitors the module voltage V_{IN} to avoid that 3.3 V drops too far and some components work beyond their operation ranges while all the other voltages are still correct.

Table 26: Trigger levels TPS3801-01

Parameter	Min.	Typ.	Max.	Unit	Remark
Trigger level (falling)	2.909	3.005	3.105	V	–40 to +85 °C
Hysteresis		15		mV	

4.3.18 Backup supply

An additional battery buffering for the RTC can be fed via the V_{BAT} pin of the module connector. A 1 kΩ resistor is switched in series between backup input of the RTC and the module connector to limit the current. To meet UL requirements a diode in series is not necessary.
In connection with a lithium battery the used RTC is UL listed.
The voltage VBAT supplies no other components except the RTC.

Table 27: Technical parameters backup input

Parameter	Min.	Typ.	Max.	Unit	Remark
Supply voltage V_{BAT}	2.97	3.30	5.50	V	
Trigger level V_{IN} V_{BAT}	2.70	2.85	2.97	V	Concerns V_{CC} of the RTC
V_{BAT}-Input current SQW/INT# activated SQW/INT# deactivated		 400 600	 700 1000	 nA nA	 Oscillator = active
V_{BAT} leakage current		25	100	nA	

<u>Sample calculation of battery service life:</u>

If a battery with a capacity of 220 mAh is used and one counts on a usable capacity of it results in the following "worst case" bridging period:

$$t_{\min}, -45..85°C = \frac{220\,mAh \cdot 67\,\%}{1\,\mu A} > 16 years$$

This shows that the bridging period will exceed the service life of the battery.
Furthermore, the backup supply is only activated when required.

5. SOFTWARE SPECIFICATION

The TQMa35 is supplied with a boot loader and a BSP for the Starterkit STK-MBa35.
More information can be found in the Support Wiki for the TQMa35.

6. MECHANICS SPECIFICATION

6.1 General information

Dimensions (W × D):	54 × 44 mm^2
Mounting holes:	None
Maximum stack height:	See Illustration 18
Component placement:	Double-sided SMD component placement
Connection with the carrier board:	SMD connector (pitch: 0.8 mm)
Board to board distance:	Selectable by different mating plugs (standard: 5.0 mm)

6.2 Dimensions and stacks heights

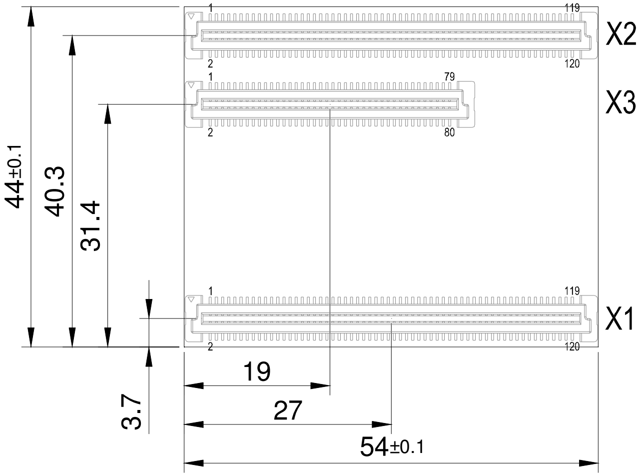


Illustration 17: Overall dimensions (top view through board)

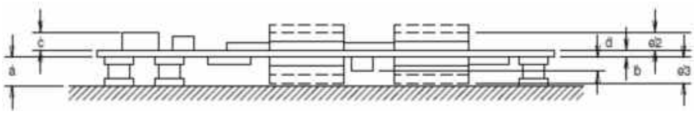


Illustration 18: Stacks heights (not to scale)

Table 28: Height dimensions

Dim.	Value [mm]	Remark
a	5.00 ± 0.20	Combination module connector with mating plug; 6, 7 and 8 mm are also possible with different connectors on carrier board
b	1.34	PC-board
c	Max. 2.54	Crystal oscillator (G2)
d	Max. 1.99	RS232 Interface converter (D3)
e2	Max. 1.60	Processor (D10)

6.3 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa35 may only be extracted from the carrier board by using the extraction tool MOZI8XXL that can also be obtained separately.

Attention: Note with respect to the component placement of the carrier board	
	2.5 mm should be kept free on the carrier board, along the longitudinal edges on both sides of the module for the extraction tool MOZI8XXL.

6.4 Component placement

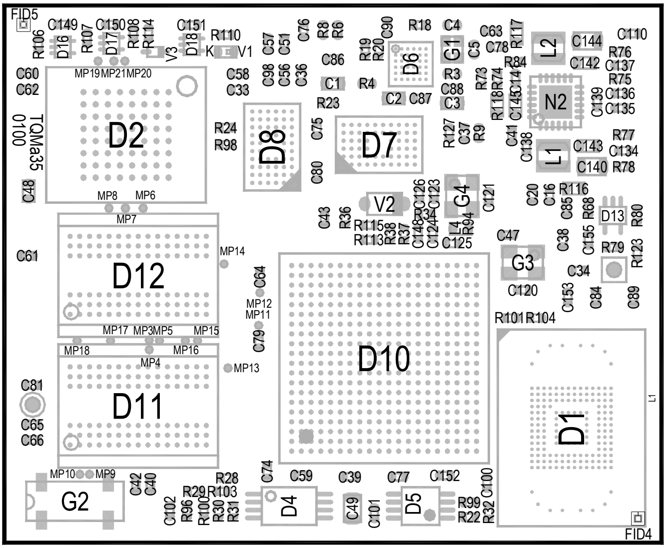


Illustration 19: Component placement top

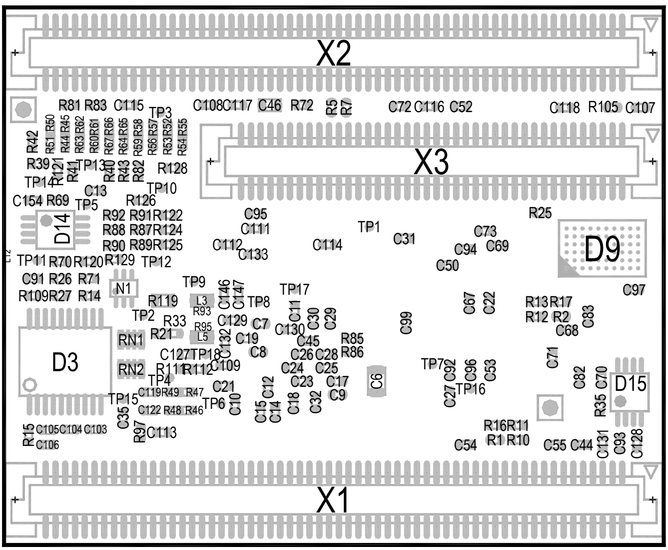


Illustration 20: Component placement bottom

6.5 Requirements for the higher-level system

6.5.1 Protection against external effects

As an embedded module it is not protected against dust, external impact and contact (IP00), an adequate form of protection has to be guaranteed by the surrounding system.

6.5.2 Thermal management

Depending on the size of memory up to 3.3 W have to be dissipated to cool the TQMa35.
The power dissipation originates primarily in the processor and in the mDDR SDRAM.
The user is responsible for the removal of this power dissipation in his application.
In most cases a passive cooling should be sufficient. In a warm environment (above approx. 40 °C) it can be necessary, to install the TQMa35 "on end" (module connectors vertical), to enable a flow of air on both sides of the module for passive cooling.

Attention: Destruction or malfunction!	
	The CPU belongs to a performance category with which in certain applications cooling can become necessary. It is the task of the user, to define a heat sink suitable for the specific case of operation (e.g., by clock frequency, stack height and airflow).

6.5.3 Structural requirements

The TQMa35 is held in the module socket by the retention force of the pins (a total of 240, resp. 320). For high requirements with respect to vibration and shock firmness an additional plastic module holder has to be provided in the final product to hold the module in its position. For this purpose TQ-Systems offers a standard solution. As no heavy and big components are used, no further requirements are given.

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC requirements

The module was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and/or shielding besides,
  notice not only the frequency, but also the signal rise times
- Filtering of all signals which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

7.2 ESD requirements

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa35. Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs
  (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, perhaps Zener diode
- Fast signal lines: Integrated protective devices (suppressor diode arrays)

7.3 Operational safety and personal security

Due to the occurring voltages (≤3.3 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Climatic and operational conditions

Permitted component temperature [11]:	0 °C to +70 °C (Commercial)
	–30 °C to +85 °C (Standard)
(Module with eMMC)	–25 °C to +85 °C
	–40 °C to +85 °C (on request)
Permitted storage temperature:	–40 °C to +100 °C
Relative air humidity (operation / storing):	10 % to 90 % (not condensing)
Protection class:	IP00

[11] Depends on placement option.

7.5 Reliability and service life

No detailed MTBF calculation has been done for the TQMa35.
It was designed to be insensitive to vibration and impact.
Middle grade connectors, which guarantee at least 100 mating cycles, were used for the module.

7.6 Environment protection

7.6.1 RoHS compliance

The TQMa35 is manufactured RoHS compliant.

- All used components and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

7.6.2 WEEE regulation

The company placing the product on the market is responsible for the observance of the WEEE regulation.
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

7.6.3 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.
The energy consumption of this subassembly is minimised by suitable measures.
Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at present there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes.
Tests or certifications regarding this were not carried out.

8. APPENDIX

8.1 References

Table 29: Further applicable documents

No.	Name	Date	Company
(1)	i.MX35 (MCIMX) Reference Manual (IMX35RM)	3/2009 – Rev. 2	Freescale
(2)	i.MX35 Data Sheet (MCIMX35SR2CEC)	4/2010 – Rev. 8	Freescale
(3)	Errata to i.MX35 Reference Manual Rev. 2 (IMX35RMAD)	5/2010 – Rev. 2.4	Freescale
(4)	Chip Errata for the i.MX35 (IMX35CE)	7/2010 – Rev. 2	Freescale
(5)	Numonyx Axcell M29EW Data sheet	5/2010	Numonyx
(6)	SN74AVCH16T245 Data sheet (SCES587B)	4/2005	Texas Instruments
(7)	DS1339 Data sheet	Rev. 100108	Maxim
(8)	STM6905 Data sheet	1/2008 – Rev. 3	ST Microelectronics
(9)	TPS3801-xx Data sheet (SLVS219C)	7/2003	Texas Instruments
(10)	LM26480 Data sheet	12/2008	National
(11)	TQMa35.Powermodes.100.pdf (Technote)	10.06.2011	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 l Gut Delling l 82229 Seefeld
info@tq-group.com l www.tq-group.com

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